TI-27832

01-25-02

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APPLICATION FOR U.S. PATENT TRANSMITTAL FORM

January 23, 2002
Box PATENT APPLICATION
Commissioner for Patents
Washington, D.C. 20231

Express Mail label number under 37 C.F.R. § 1.10:
EJ502271574US

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Dear Sir:

Transmitted herewith for filing is the patent application of:
Inventor: Potts

For: Semiconductor Wafer With Grouped Integrated Circuit Die Having Inter-Die Connections For Group Testing

Enclosed are:
(1) patent application including 31 pages of specification, 4 sheets of informal drawings, an executed Declaration and Power of Attorney;
(2) Assignment (with cover sheet) of the invention to TEXAS INSTRUMENTS INCORPORATED, P.O. Box 655474, MS3999, Dallas, Texas 75265;
(3) LETTER TO THE OFFICIAL DRAFTSPERSON with three (3) sheets of formal drawings; and
(4) Information Disclosure Statement (with Form 1449A) and the single cited patent; and
(5) Preliminary Amendment.

This application claims the benefit, under 35 U.S.C. §119(e)(1), of U.S. Provisional Application No. 60/344,161 (TI-27832PS), filed December 27, 2001.

FEE CALCULATION					FEE
				Basic Fee	740
	Number		Extra	Rate	
Total Claims	38	20	18	18	324
Independent Claims	3	3	0	84	0
				TOTAL FEES	1064

Please charge deposit account No. 20-0668 in the amount of the Total Fees set forth above. The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to said deposit account. **A duplicate copy of this sheet is enclosed.**

All correspondence regarding this application may be directed to Applicants' attorney at ***Customer number 23494***, or at the below listed telephone number and address.

Ronald O. Neerings
Texas Instruments Incorporated
P.O. Box 655474, M/S 3999
Dallas, Texas 75265
(972) 917-5299

Respectfully submitted,

Stephen L. Levine
Reg. No. 33,413

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: Potts (Attny docket: TI-27832)
Serial No. not assigned Group Art Unit: not assigned
Filed: January 23, 2002 Examiner: not assigned
For: Semiconductor Wafer With Grouped Integrated Circuit Die Having Inter-Die Connections For Group Testing

LETTER TO THE OFFICIAL DRAFTSPERSON

Box PATENT APPLICATION
Commissioner for Patents
Washington, DC 20231

Dear Sir:

Transmitted herewith are three (3) sheets of the formal drawings for the above-referenced application, for replacement of those filed with the enclosed application.

The Patent and Trademark Office is requested to telephone the undersigned in the event of any questions regarding the enclosed drawings.

Respectfully submitted,

Anderson, Levine & Lintel, L.L.P.
12160 Abrams Road, Suite 111
Dallas, Texas 75243-4523
(972) 664-9552

Stephen L. Levine
Registry No. 33,413
Attorney for Applicant

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